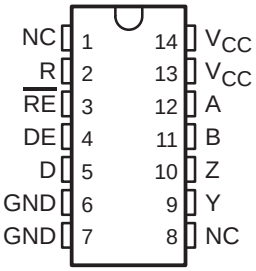
SLLS052E – AUGUST 1987 – REVISED OCTOBER 1998

- **Meet or Exceed the Requirements of TIA/EIA-422-B, TIA/EIA-485-A† and ITU Recommendation V.11**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 25-MBaud Operation in Both Serial and Parallel Applications**
- **Low Skew Between Devices . . . 6 ns Max**
- **Low Supply-Current Requirements . . . 30 mA Max**
- **Individual Driver and Receiver I/O Pins With Dual V_{CC} and Dual GND**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive- and Negative-Current Limiting**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 60 mV Typ**
- **Operate From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**

D OR N PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN65ALS180 and SN75ALS180 differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. They are designed for balanced transmission lines and meet TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11.

The SN65ALS180 and SN75ALS180 combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate terminals for greater flexibility and are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0.

These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The SN65ALS180 is characterized for operation from –40°C to 85°C. The SN75ALS180 is characterized for operation from 0°C to 70°C.

† These devices meet or exceed the requirements of TIA/EIA-485-A, except for the Generator Contention Test (para. 3.4.2) and the Generator Current Limit (para. 3.4.3). The applied test voltage ranges are –6 V to 8 V for the SN75ALS180 and –4.5 V to 8 V for the SN65ALS180.

Function Tables

DRIVER

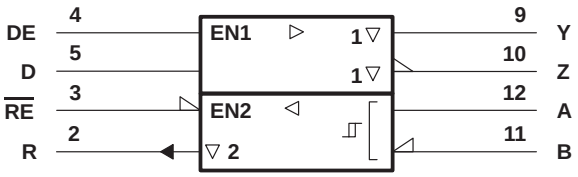
INPUT D	ENABLE DE	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

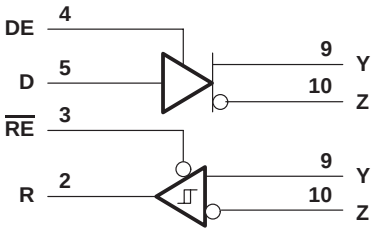
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol†



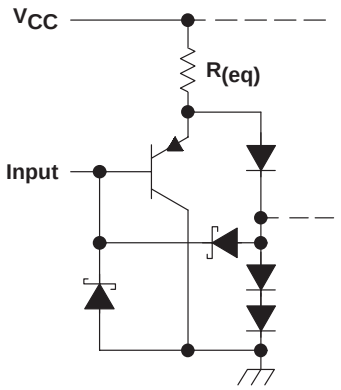
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



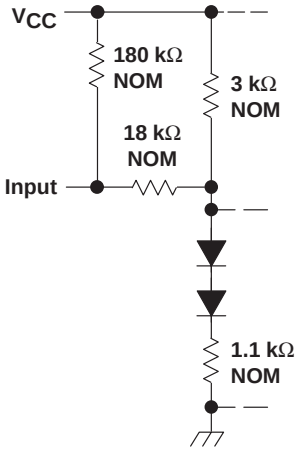
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

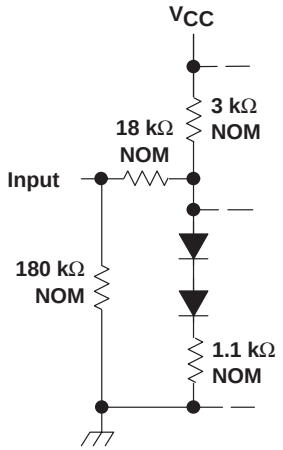


Driver and Driver Enable Inputs: $R_{(eq)}$ = 12 kΩ NOM
Receiver Enable Input: $R_{(eq)}$ = 30 kΩ NOM
$R_{(eq)}$ = Equivalent Resistor

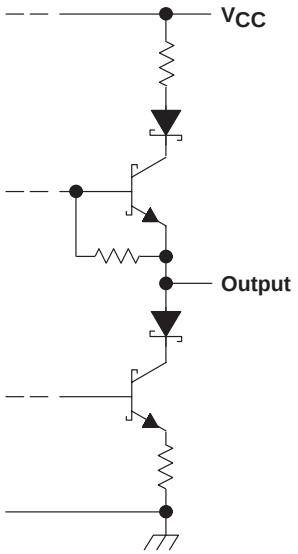
RECEIVER A INPUT



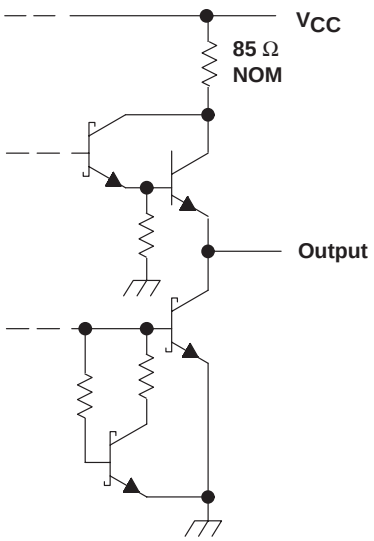
RECEIVER B INPUT



DRIVER OUTPUT



TYPICAL OF RECEIVER OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage range at any bus terminal . . . . . –10 V to 15 V
Enable input voltage, V_I . . . . . 5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 127°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{st} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				–7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 3)				±12	V
High-level output current, I_{OH}	Driver			–60	mA
	Receiver			–400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65ALS180	–40		85	°C
	SN75ALS180	0		70	

NOTE 3: Differential-input/output bus voltage is measured at the noninverting terminal, A/Y, with respect to the inverting terminal, B/Z.

DRIVERS

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1} or 2§			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	
V_{OD3}	Differential output voltage	V_{test} = –7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage¶	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage¶					±0.2	V
I_O	Output current	Output disabled, See Note 4	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current#	V_O = –6 V	SN75ALS180			–250	mA
		V_O = –4 V	SN65ALS180			–250	
		V_O = 0	All			–150	
		V_O = V_{CC}	All				
		V_O = 8 V	All				
I_{CC}	Supply current	No load	Driver outputs enabled, Receiver disabled		25	30	mA
			Outputs disabled		19	26	

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.
¶ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
# Duration of the short circuit should not exceed one second for this test.
NOTE 4: This applies for both power on and off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	C_L = 50 pF,	See Figure 3	3	8	13	ns
	Pulse skew ($\|t_{d(ODH)} - t_{d(ODL)}\|$)					1	6	ns
$t_{t(OD)}$	Differential output transition time				3	8	13	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4			23	50	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5			19	24	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4			8	13	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5			8	13	ns

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (test termination measurement 2)
V_{test}		V_{tst}
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVERS

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA		–0.2‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					60		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA					–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –400 μA,	See Figure 6	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV,	I_{OL} = 8 mA,	See Figure 6			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input = 0 V, See Note 5	V_I = 12 V				1	mA
			V_I = –7 V				–0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					–100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0		–15		–85	mA
I_{CC}	Supply current	No load	Receiver outputs enabled, Driver inputs disabled			19	30	mA
			Outputs disabled			19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 5: This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = –1.5 V to 1.5 V, See Figure 7	C_L = 15 pF,	9	14	19	ns
t_{PHL}	Propagation delay time, high- to low-level output			9	14	19	ns
	Skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 8		7	14	ns
t_{PZL}	Output enable time to low level				7	14	ns
t_{PHZ}	Output disable time from high level				20	35	ns
t_{PLZ}	Output disable time from low level				8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

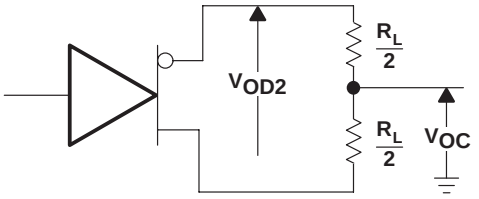


Figure 1. Driver V_{OD} and V_{OC}

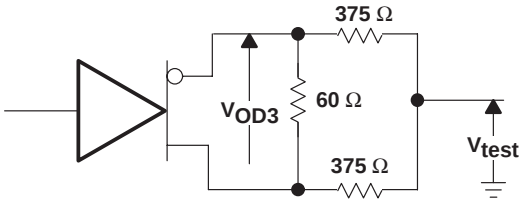
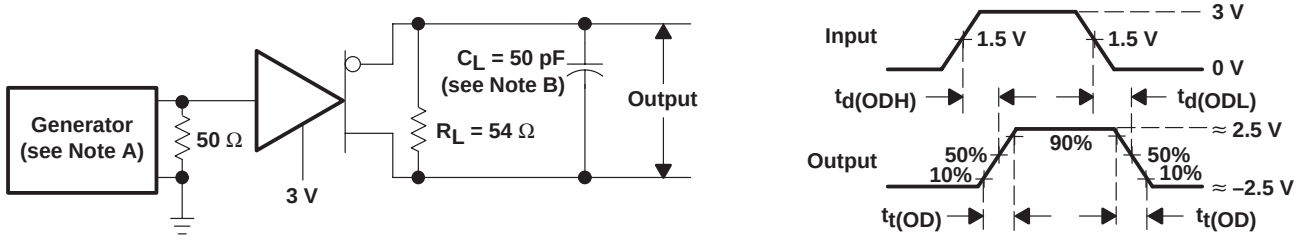


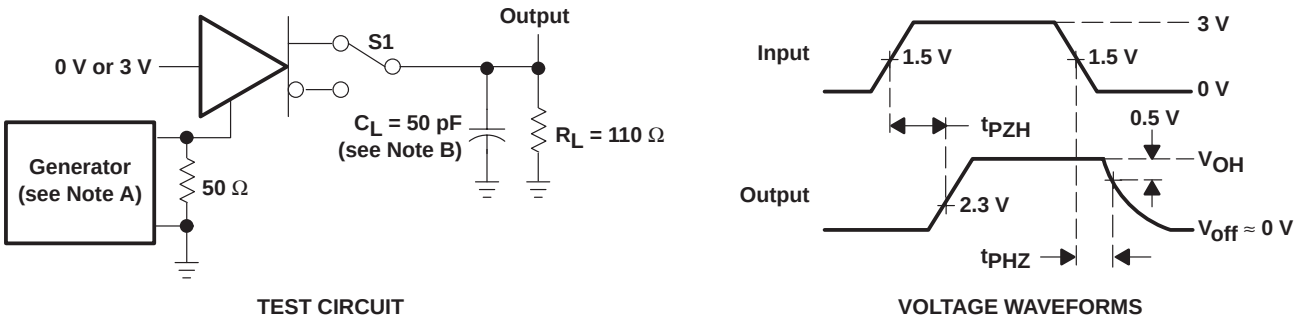
Figure 2. Driver V_{OD3}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

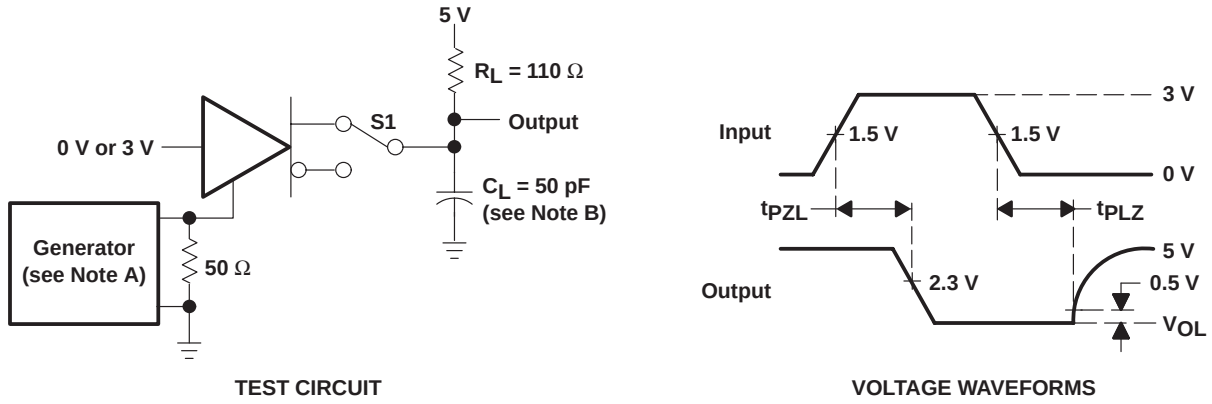
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms

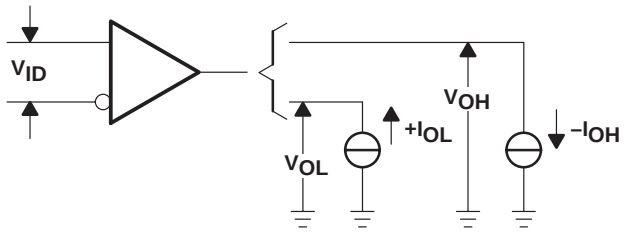
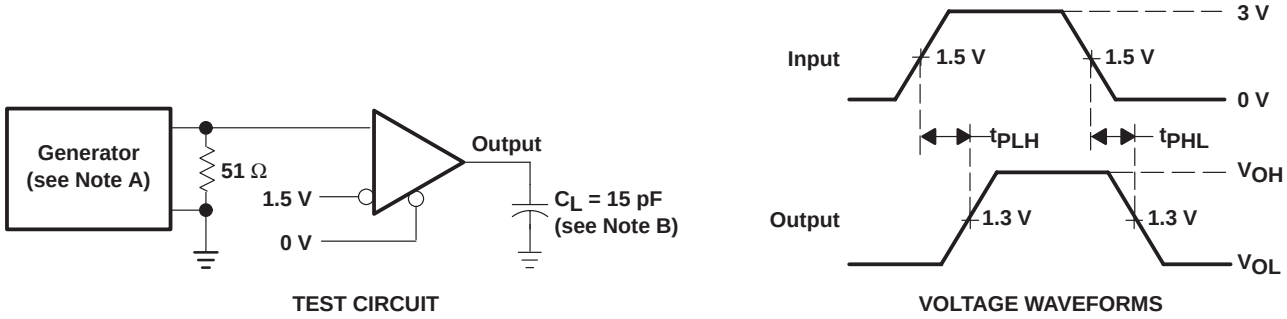


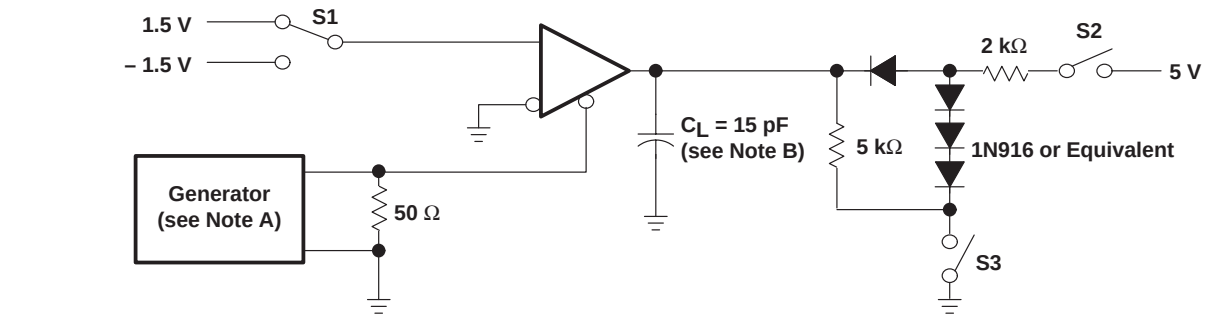
Figure 6. Receiver V_{OH} and V_{OL}

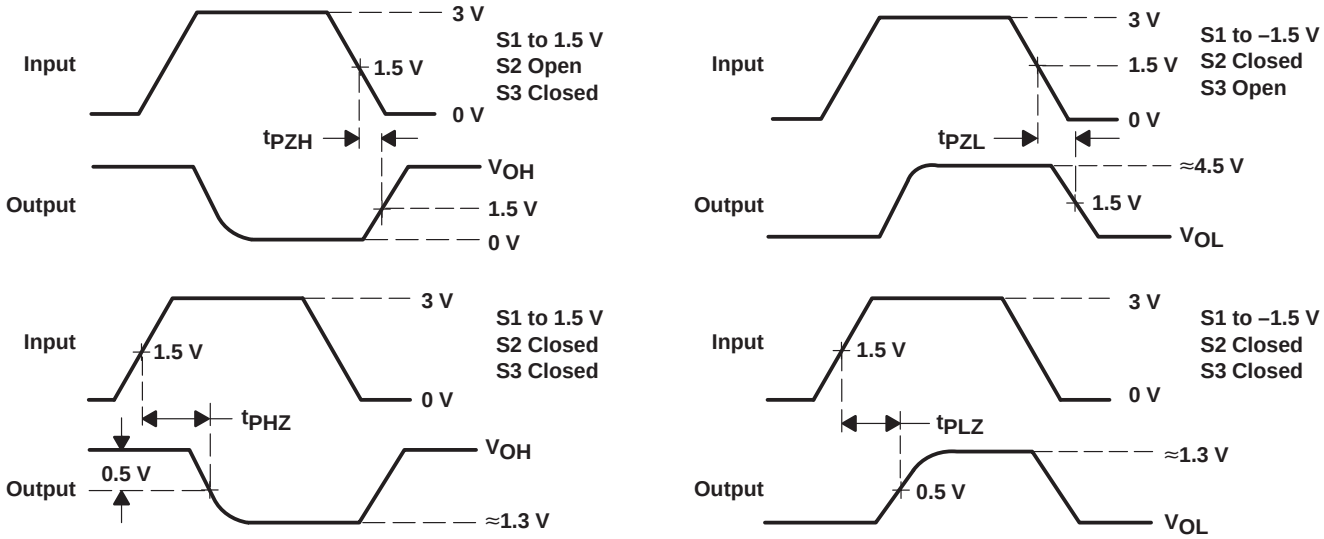
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms





NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 8. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS – DRIVERS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

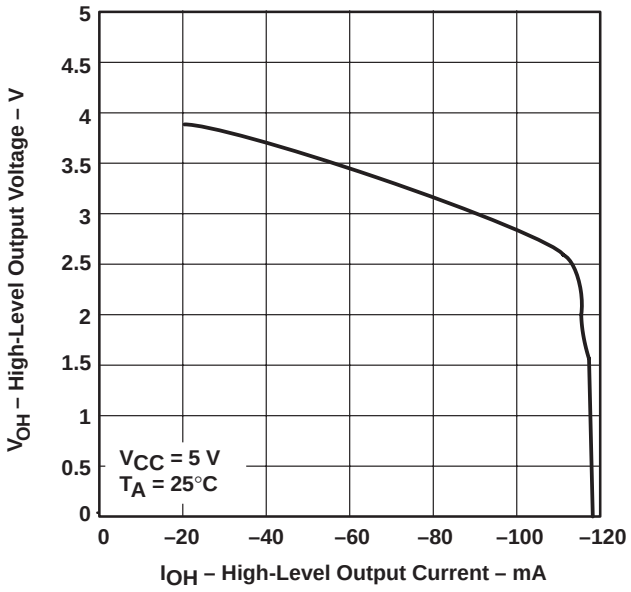


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

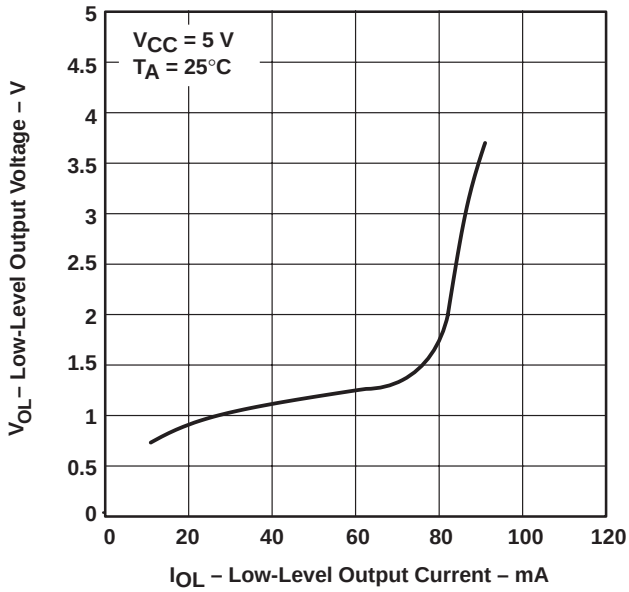


Figure 10

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

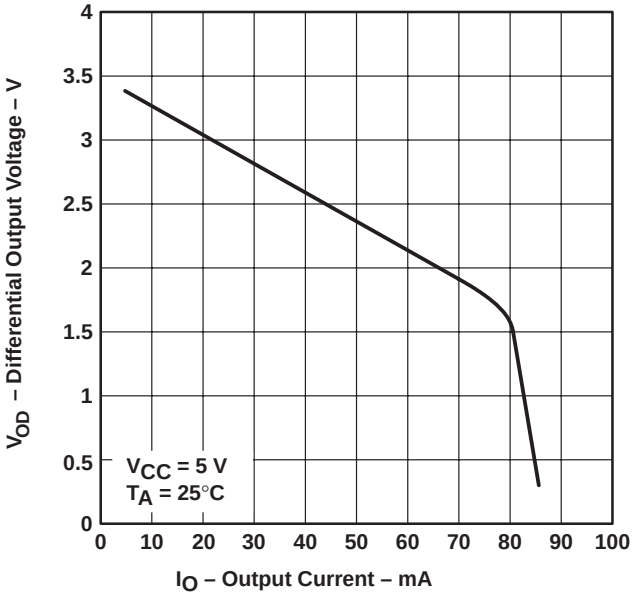


Figure 11

TYPICAL CHARACTERISTICS – RECEIVERS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

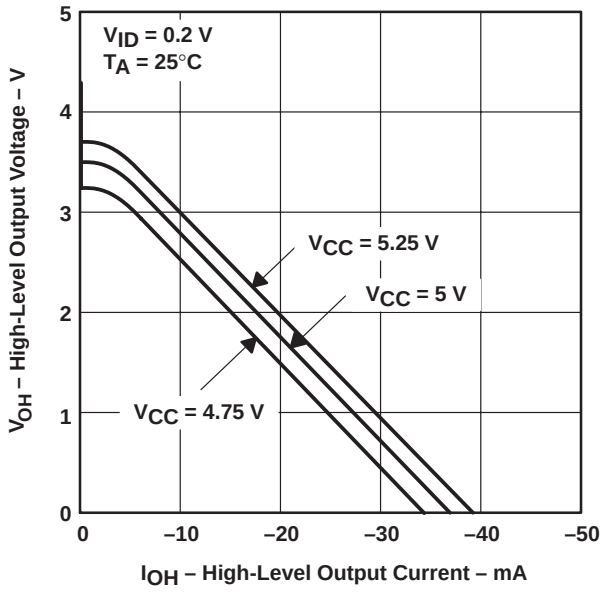


Figure 12

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

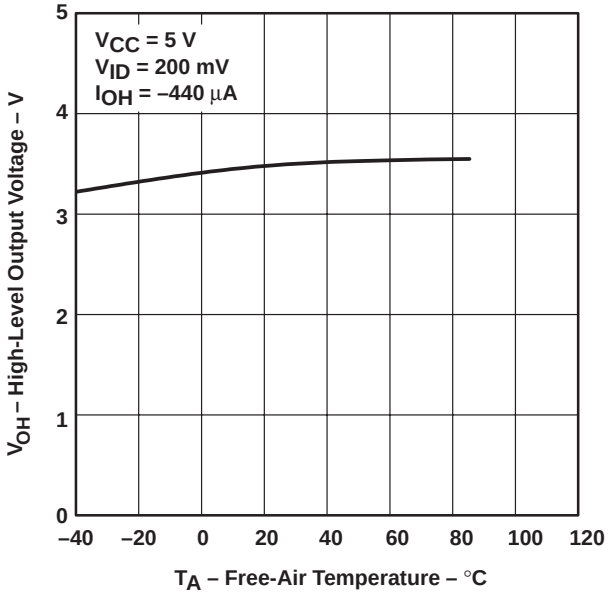


Figure 13

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

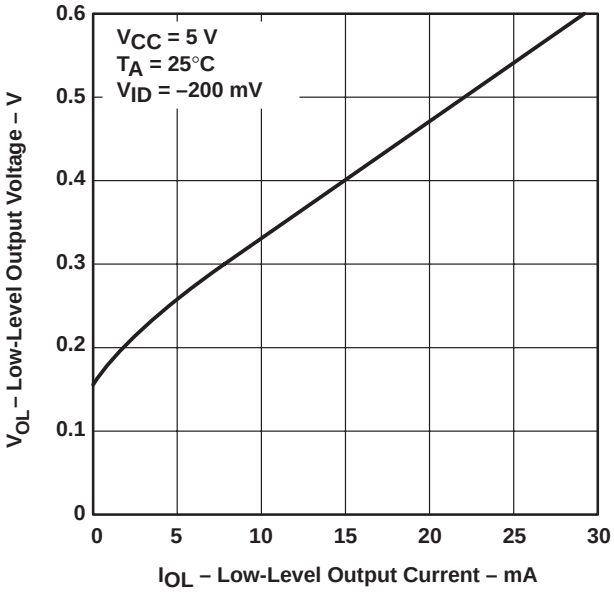


Figure 14

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

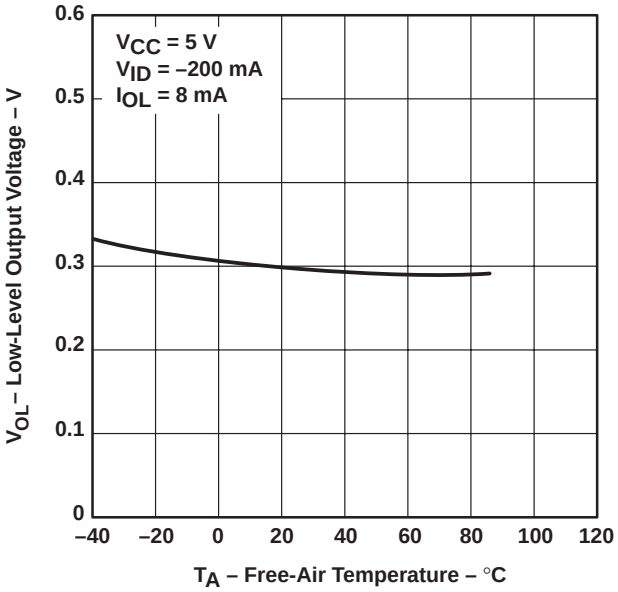


Figure 15

TYPICAL CHARACTERISTICS – RECEIVERS

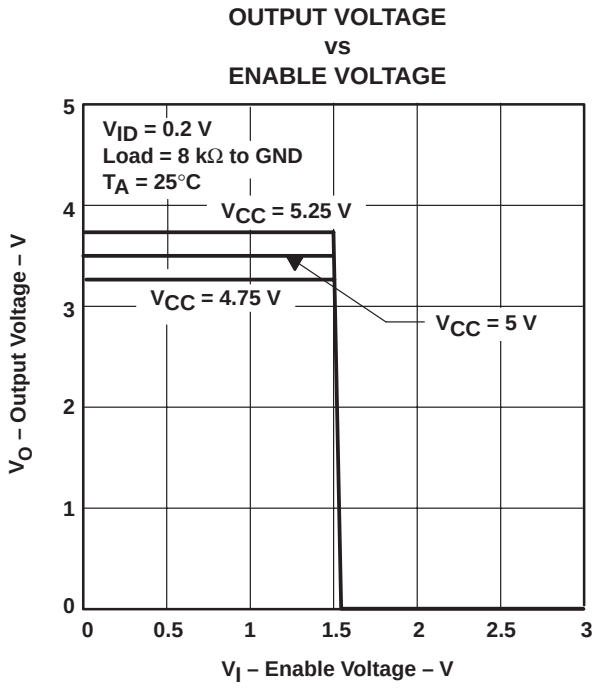


Figure 16

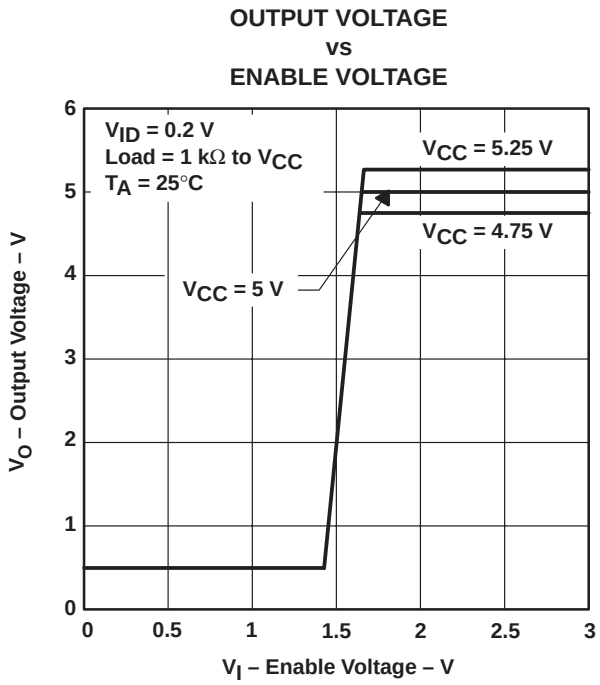
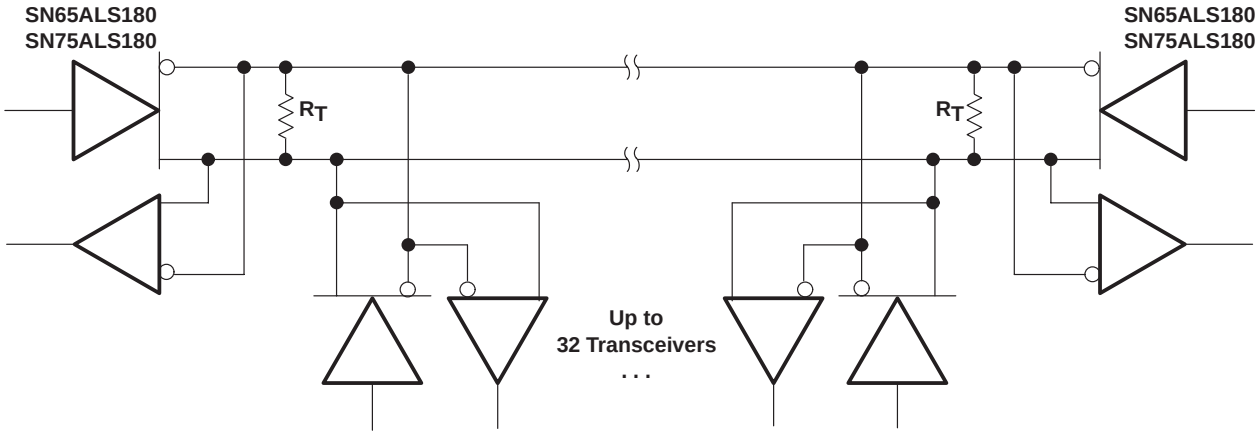


Figure 17

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

IMPORTANT NOTICE

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