

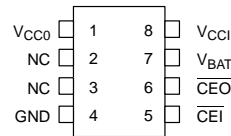
DALLAS
SEMICONDUCTOR

DS1218 Nonvolatile Controller

FEATURES

- Converts CMOS RAM into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- Space saving 8-pin mini-DIP/8-pin 150 mil SOIC
- Consumes less than 100 na of battery current

PIN ASSIGNMENT



PIN DESCRIPTION

V_{CCI}	-	Input +5 Volt Supply
V_{CCO}	-	RAM Power (V_{CC}) Supply
\overline{CEI}	-	Chip Enable Input
NC	-	No Connection
\overline{CEO}	-	Chip Enable Output
V_{BAT}	-	+ Battery
GND	-	Ground

DESCRIPTION

The DS1218 is a CMOS circuit which solves the application problems of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, the chip enable output is inhibited to accomplish write protection and the battery is switched on to supply RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8-pin mini-DIP package keeps PC board real estate requirements to a minimum. By combining the DS1218 nonvolatile controller chip with a full CMOS memory and lithium batteries, ten years of nonvolatile RAM operation can be achieved.

OPERATION

The DS1218 Nonvolatile Controller performs the circuit functions required to battery back up a RAM. First, a

switch is provided to direct power from the battery or V_{CCI} supply depending on which is greater. This switch has a voltage drop of less than 0.2V. The second function which the nonvolatile controller provides is power fail detection. The DS1218 constantly monitors the V_{CC} supply. When V_{CCI} falls to 1.26 times the battery voltage a precision comparator outputs a power fail detect signal to the chip enable logic. The third function of write protection is accomplished by holding the chip enable output signal to within 0.2V of the V_{CCI} or battery supply, when a power fail condition is detected.

During nominal supply conditions, the chip enable output will follow chip enable input with a maximum propagation delay of 10 ns.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply	V _{CCI}	4.5	5.0	5.5	V	1
Logic 1	V _{IH}	2.0		5.5	V	1
Logic 0	V _{IL}	-0.3		0.8	V	1
Battery Supply	V _{BAT}	2.5	3.0	3.5	V	1

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; V_{CCI} = 5V ± 10%)

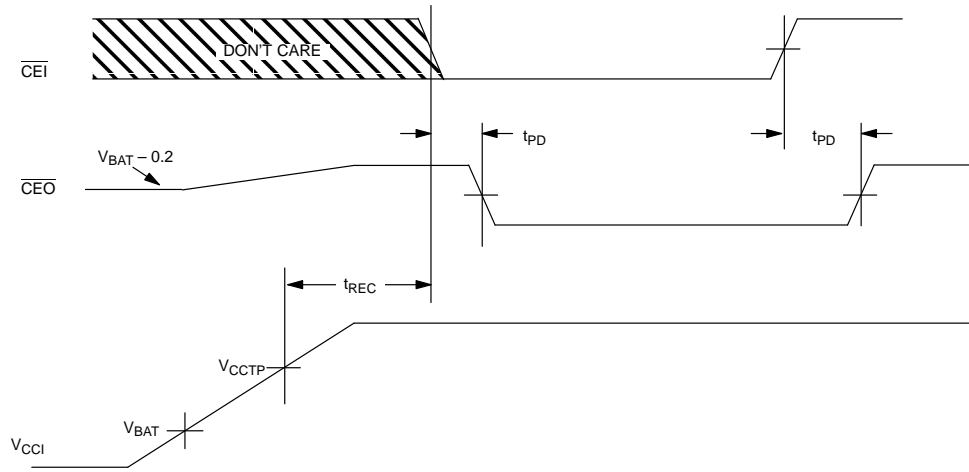
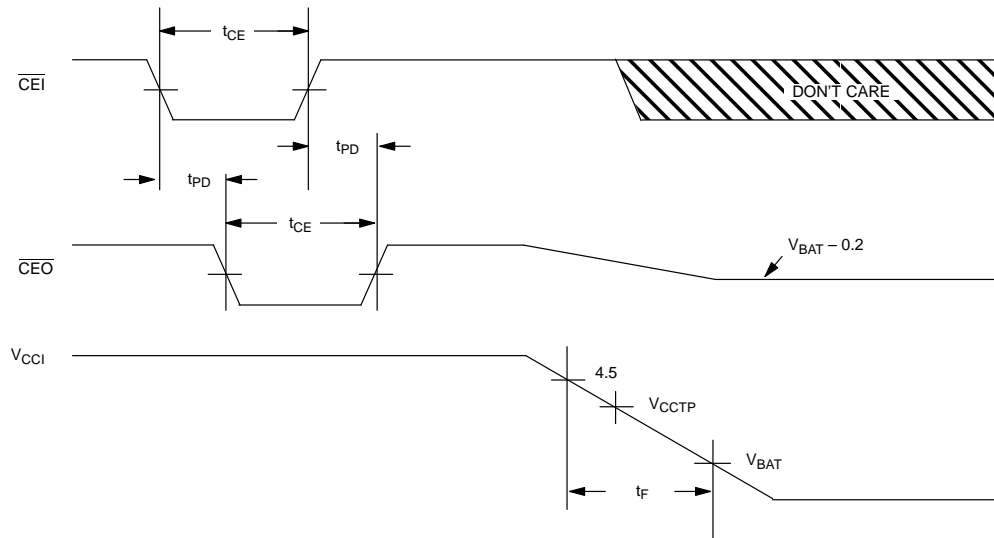
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Current	I _{CCI}		2	5	mA	3
Battery Current	I _{BAT}			100	nA	3, 4
RAM Current (V _{CCO1} ≥ V _{CCI} - 0.3V)	I _{CCO}			80	mA	5
RAM Current (V _{CCO} ≥ V _{CCI} - 0.2V)	I _{CCO}		70		mA	
Input Leakage	I _{IL}	-1.0		+1.0	μA	
CE ₀ Output @ 2.4V	I _{OH}	-1.0			mA	
CE ₀ Output @ 0.4V	I _{OL}			4.0	mA	
V _{CC} Trip Point	V _{CCTP}		1.26XV _{BAT}			

CAPACITANCE(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C _{IN}			5	pF	
Output Capacitance	C _{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE Propagation Delay	t _{PD}		4	10	ns	2
Recovery at Power-Up	t _{REC}	0.2		2	ms	
V _{CC} Slew Rate	t _F	500			μs	
CE Pulse Width	t _{CE}			1.5	μs	6, 7

TIMING DIAGRAM: POWER UP**TIMING DIAGRAM: POWER DOWN**

NOTES:

1. All voltages referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Outputs open.
4. Drain from battery when $V_{CC} < V_{BAT}$.
5. Maximum amount of current which can be drawn through pin 1 of the controller.
6. $t_{CE\ max}$ must be met to ensure data integrity on power loss.
7. $\overline{CE\ O}$ can only sustain leakage current in the battery backup mode.

OUTPUT LOAD Figure 1