Programming and Interfacing the 8051 Microcontroller in C and Assembly

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CHAPTER 1

ARCHITECTURE

1.1. Microprocessors and Microcontrollers

A digital computer typically consists of three major components: the Central Processing Unit (CPU), program and data memory, and an Input/Output (I/O) system. The CPU controls the flow of information among the components of the computer. It also processes the data by performing digital operations. Most of the processing is done in the Arithmetic-Logic Unit (ALU) within the CPU. When the CPU of a computer is built on a single printed circuit board, the computer is called a minicomputer. A microprocessor is a CPU that is compacted into a single-chip semiconductor device. Microprocessors are general-purpose devices, suitable for many applications. A computer built around a microprocessor is called a microcomputer. The choice of I/O and memory devices of a microcomputer depends on the specific application. For example, most personal computers contain a keyboard and monitor as standard input and output devices.

A microcontroller is an entire computer manufactured on a single chip. Microcontrollers are usually dedicated devices embedded within an application. For example, microcontrollers are used as engine controllers in automobiles and as exposure and focus controllers in cameras. In order to serve these applications, they have a high concentration of on-chip facilities such as serial ports, parallel input-output ports, timers, counters, interrupt control, analog-to-digital converters, random access memory, read only memory, etc. The I/O, memory, and on-chip peripherals of a microcontroller are selected depending on the specifics of the target application. Since microcontrollers are powerful digital processors, the degree of control and programmability they provide significantly enhances the effectiveness of the application.

Embedded control applications also distinguish the microcontroller from its relative, the general-purpose microprocessor. Embedded systems often require real-time operation and multitasking capabilities. Real-time operation refers to the fact that the embedded controller must be able to receive and process the signals from its environment as they are received. That is, the environment must not wait for the controller to become available. Similarly, the controller must perform fast enough to output control signals to its environment when they are needed. Again, the environment must not wait for the controller. In other words, the embedded controller should not be a bottleneck in the operation of the system. Multitasking is the capability to perform many functions in a simultaneous or quasi-simultaneous manner.

The embedded controller is often responsible of monitoring several aspects of a system and responding accordingly when the need arises.

The 8051 is the first microcontroller of the MCS-51 family introduced by Intel Corporation at the end of the 1970s. The 8051 family with its many enhanced members enjoys the largest market share, estimated to be about 40%, among the various microcontroller architectures. The architecture of the 8051 family of the microcontrollers is presented in this chapter. First, the original 8051 microcontroller is discussed, followed by the enhanced features of the 8032, and the 80C515.

1.2. The 8051 Microcontroller Family Architecture

The architecture of the 8051 family of microcontrollers is referred to as the MCS-51 architecture, or sometimes simply as MCS-51. The microcontrollers have an 8-bit data bus. They are capable of addressing 64K of program memory and a separate 64K of data memory. The 8051 has 4K of code memory implemented as on-chip *Read Only Memory* (ROM). The 8051 has 128 bytes of internal *Random Access Memory* (RAM). The 8051 has two timer/counters, a serial port, 4 general purpose parallel input/output ports, and interrupt control logic with five sources of interrupts. Besides internal RAM, the 8051 has various *Special Function Registers* (SFR), which are the control and data registers for on-chip facilities. The SFRs also include the accumulator, the B register, and the *Program Status Word* (PSW), which contains the CPU flags. Programming the various internal hardware facilities of the 8051 is achieved by placing the appropriate control words into the corresponding SFRs. The 8031 is similar to the 8051, except it lacks the on-chip ROM.

As stated, the 8051 can address 64K of external data memory and 64K of external program memory. These may be separate blocks of memory, so that up to 128K of memory can be attached to the microcontroller. Separate blocks of code and data memory are referred to as the Harvard architecture. The 8051 has two separate read signals, RD# (P3.7) and PSEN#. The first is activated when a byte is to be read from external data memory, the other, from external program memory. Both of these signals are so-called active low signals. That is, they are cleared to logic level 0 when activated. All external code is fetched from external program memory. In addition, bytes from external program memory may be read by special read instructions such as the MOVC instruction. There are separate instructions to read from external data memory, such as the MOVX instruction. That is, the instructions determine which block of memory is addressed, and the corresponding control signal, either RD# or PSEN# is activated during the memory read cycle. A single block of memory may be mapped to act as both data and program memory. This is referred to as the Von Neumann[1] architecture. In order to read from the same block using either the RD#

[1] Named after John Von Neumann, a prolific mathematician and computer scientist of the 20th century.

signal or the PSEN# signal, the two signals are combined with a logic AND operation. This way, the output of the AND gate is low when either input is low. The advantage of the Harvard architecture is not simply doubling the memory capacity of the microcontroller. Separating program and data increases the reliability of the microcontroller, since there are no instructions to write to the program memory. A ROM device is ideally suited to serve as program memory. The Harvard architecture is somewhat awkward in evaluation systems, where code needs to be loaded into program memory. By adopting the Von Neumann architecture, code may be written to memory as data bytes, and then executed as program instructions.

The 8052 has 256 bytes of internal RAM and 8K of internal code ROM. The 8051 and 8052 internal ROM cannot be programmed by the user. The user must supply the program to the manufacturer, and the manufacturer programs the microcontrollers during production. Due to the setup costs, the factory masked ROM option is not economical for small quantity productions. The 8751 and 8752 are the *Erasable Programmable Read Only Memory* (EPROM) versions of the 8051 and 8052. Many manufacturers offer the EPROM versions in windowed ceramic and non-windowed plastic packages. These are user programmable. However, the non-windowed versions cannot be erased. These are usually referred to as One-Time-Programmable (OTP) microcontrollers, which are more suitable for experimental work or for small production runs. The 8951 and 8952 contain FLASH EEPROMs (Electrically Erasable Programmable Read Only Memory). These chips can be programmed as the EPROM versions, using a chip programmer. Moreover, the memory may be erased. Similar to EPROMs, Erasing FLASH memory sets all data bits (data bytes become FFh). A bit may be cleared (made 0) by programming. However, a zero bit may not be programmed to a one. This requires erasing the chip. Some larger FLASH memories are organized in banks or sectors. Rather than erasing the entire chip, you may erase a given sector and keep the remaining sectors unchanged.

During the past decade, many manufacturers introduced enhanced members of the 8051 microcontroller. The enhancements include more memory, more ports, analog-to-digital converters, more timers with compare, reload and capture facilities, more interrupt sources, higher precision multiply and divide units, idle and power down mode support, watchdog timers, and network communication subsystems. All microcontroller of the family use the same set of machine instructions, the MCS-51. The enhanced features are programmed and controlled by additional SFRs. In the remainder of this chapter, the hardware architecture of the 8051 is presented. The enhancements brought by the 8052 and 80C515 follow. Some of the more popular enhanced members of the family are reviewed at the end of Chapter 2. The reader is referred to the manufacturers' data books for the specifics of other enhanced members.

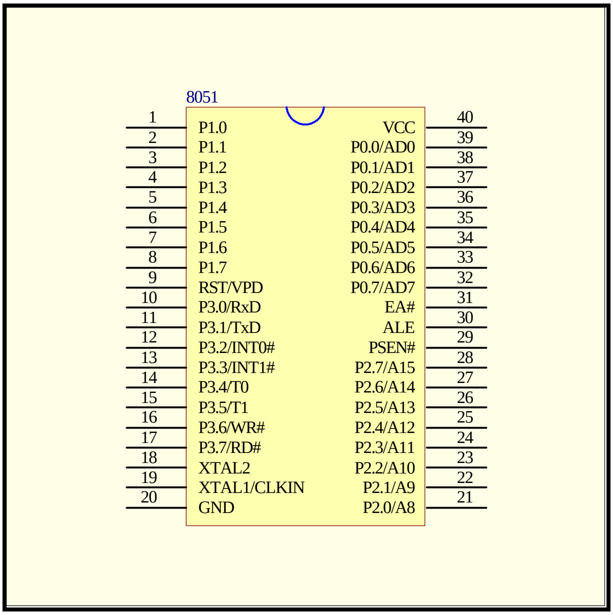

Figure 1.1. Pinout of the 8051 Microcontroller (NC stands for No Connection).

If the program fits into the on-chip ROM and if the internal RAM is sufficient, the MCS-51 family of microcontrollers requires no additional logic to implement a complete controller system. The following discusses the 8051 in detail.

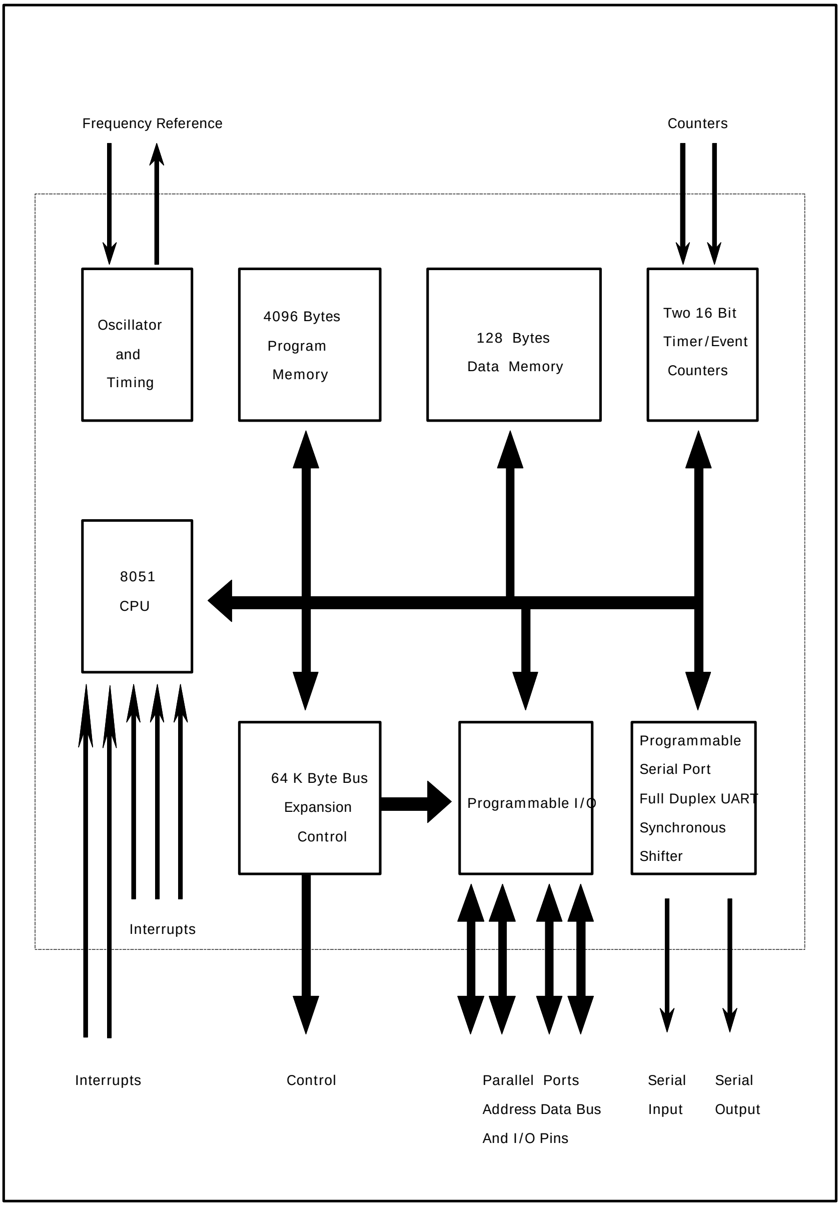
Frequency Reference
Counters
Oscillator and Timing
4096 Bytes Program Memory
128 Bytes Data Memory
Two 16 Bit Timer/Event Counters
8051 CPU
64 K Byte Bus Expansion Control
Programmable I/O
Programmable Serial Port Full Duplex UART Synchronous Shifter
Interrupts
Interrupts
Control
Parallel Ports Address Data Bus And I/O Pins
Serial Input
Serial Output

Figure 1.2. The Block Diagram of the 8051 Microcontroller.